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pureCOLD fast electronics for β-α pile-up suppression first on-line measurements

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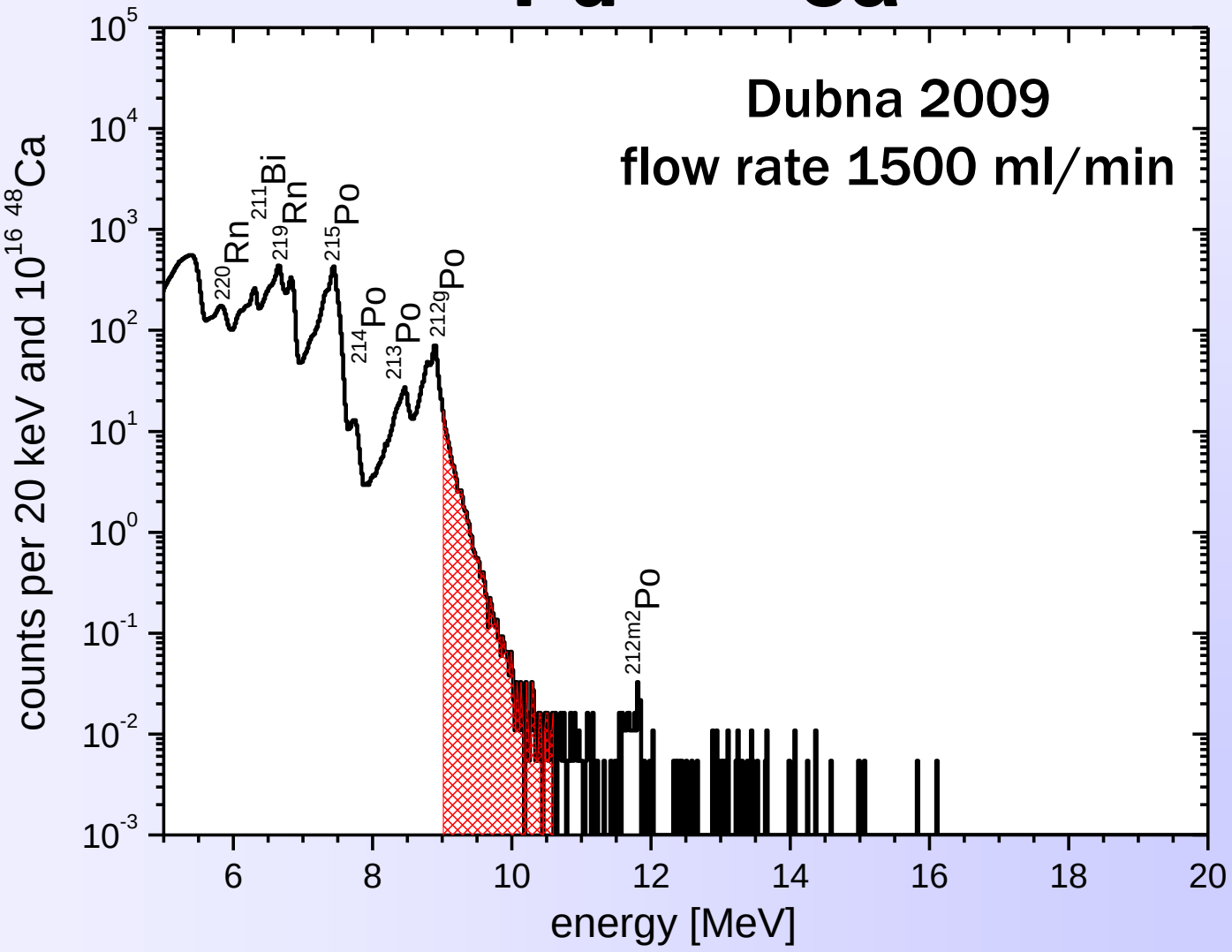
Peter Rasmussen

Pile-Up Rejection Electronics for Cryo On-Line Detector **pureCOLD**

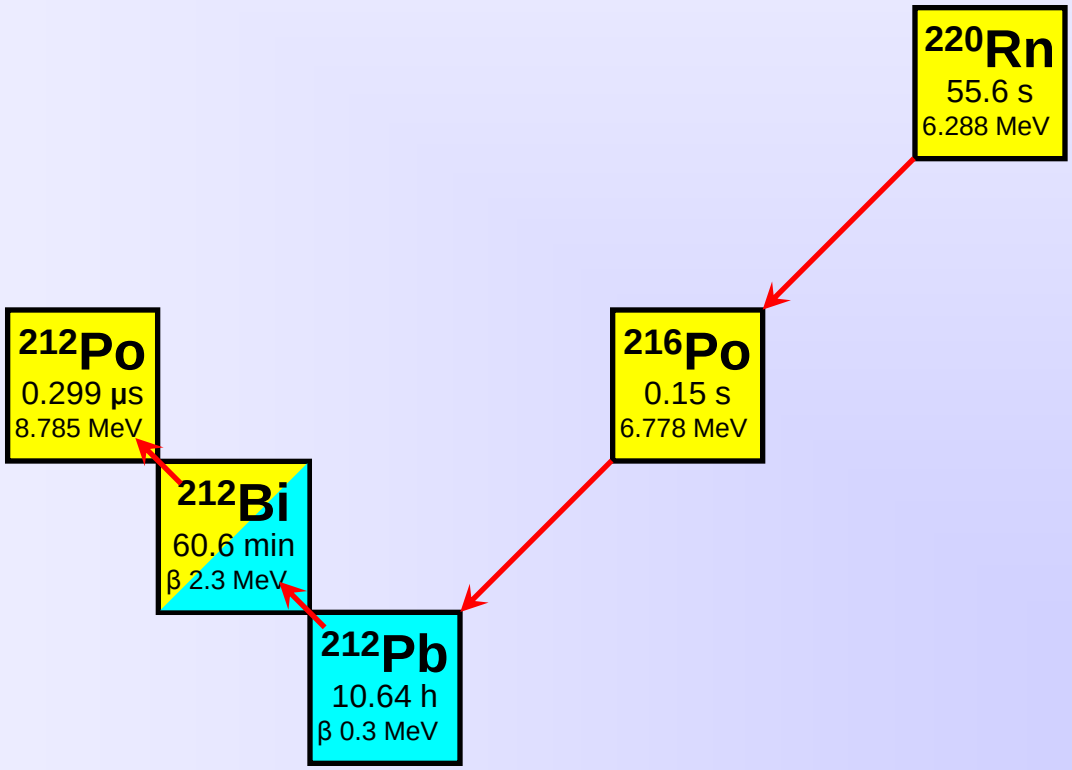
Outline

- Introduction
- Final hardware design
- Measurements PSI & Dubna 2011
- Summary & Outlook

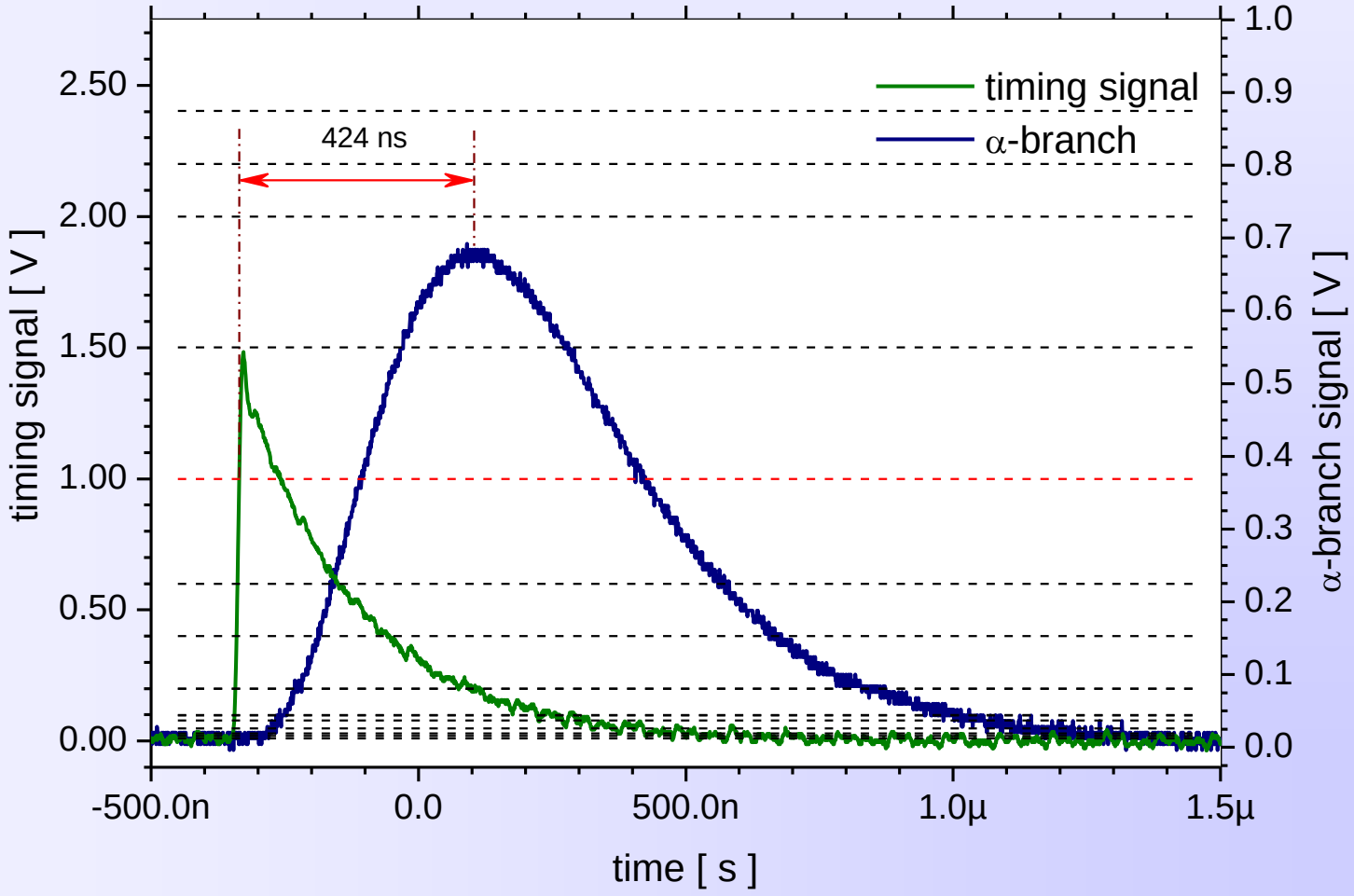
α-Spectrum
$^{242}Pu + ^{48}Ca$



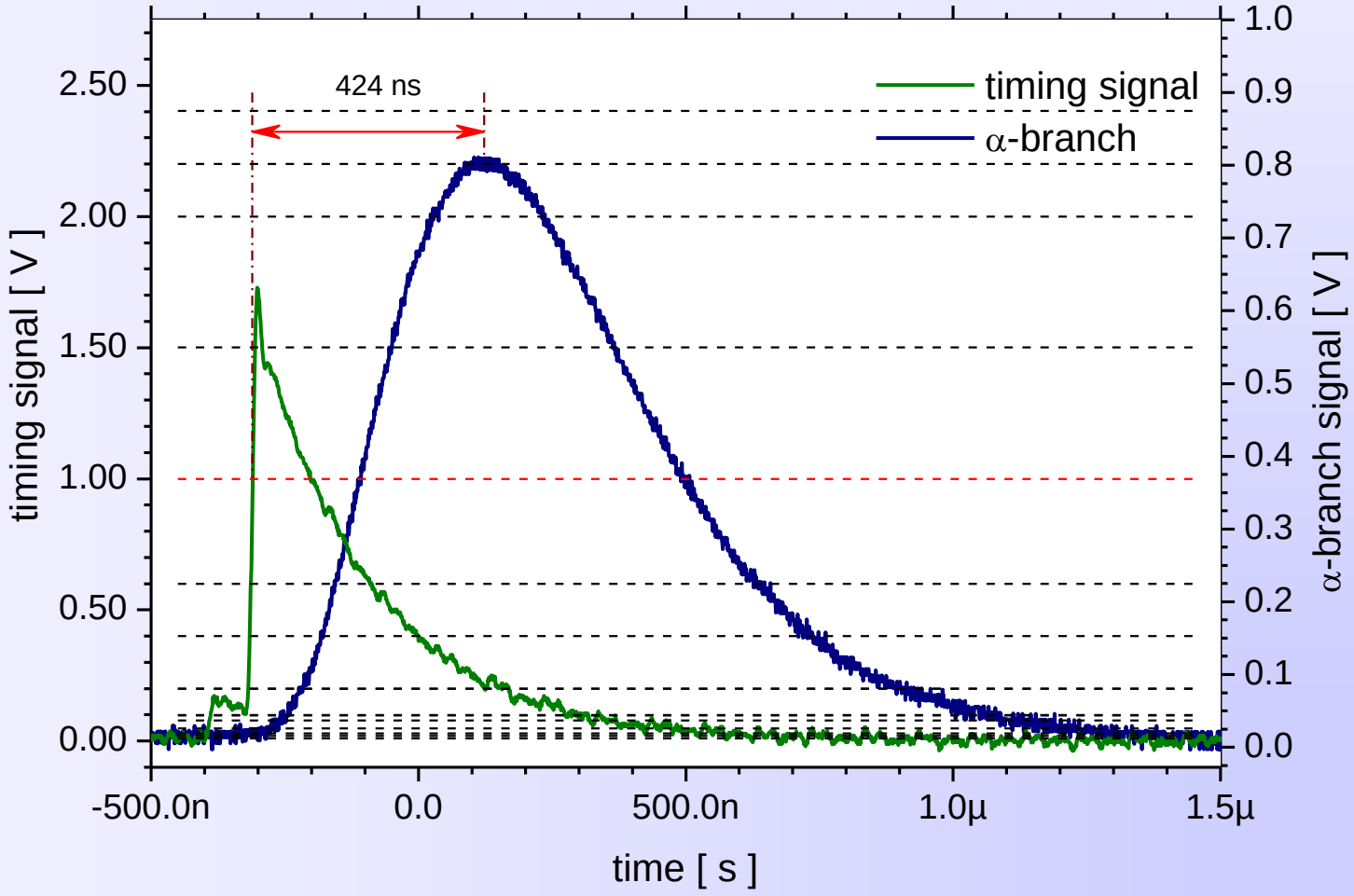
β-α Pile-Up Problem



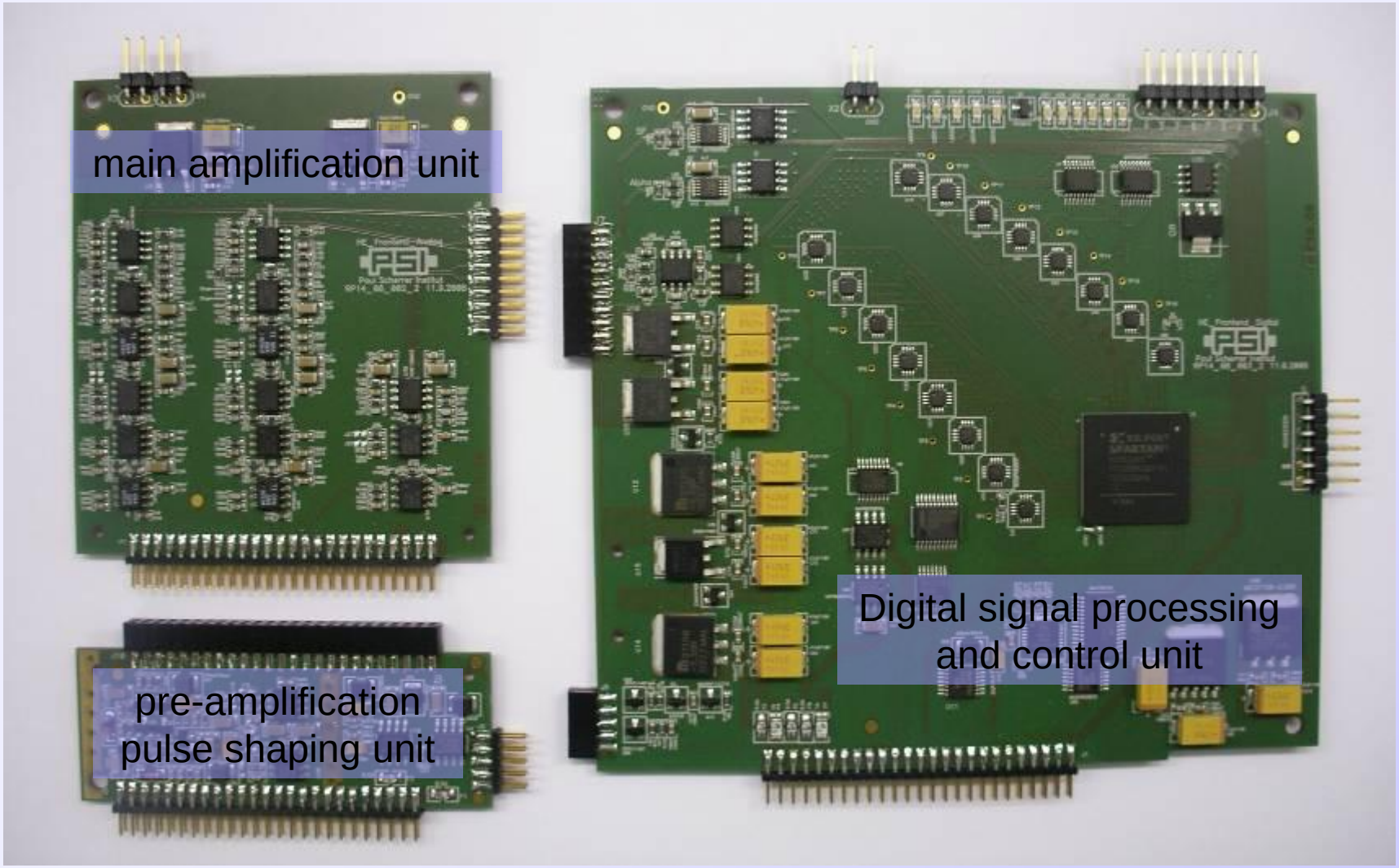
Working Principle
pure α-Event



Working Principle
β-α Pile-Up Event

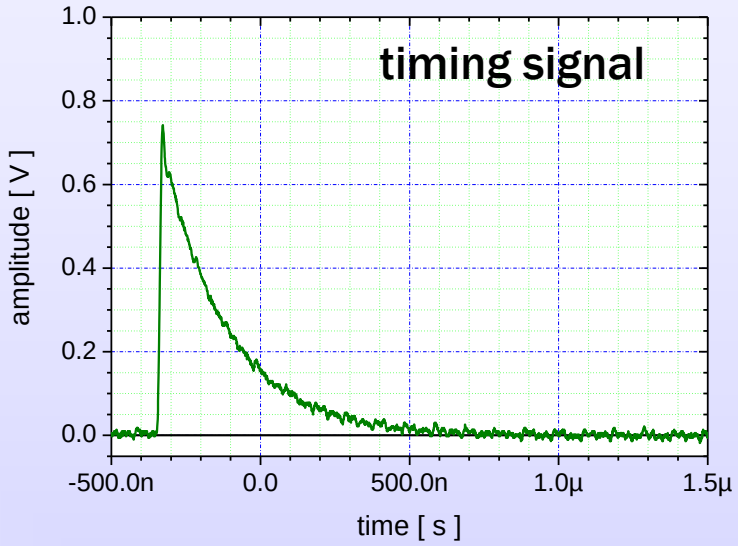


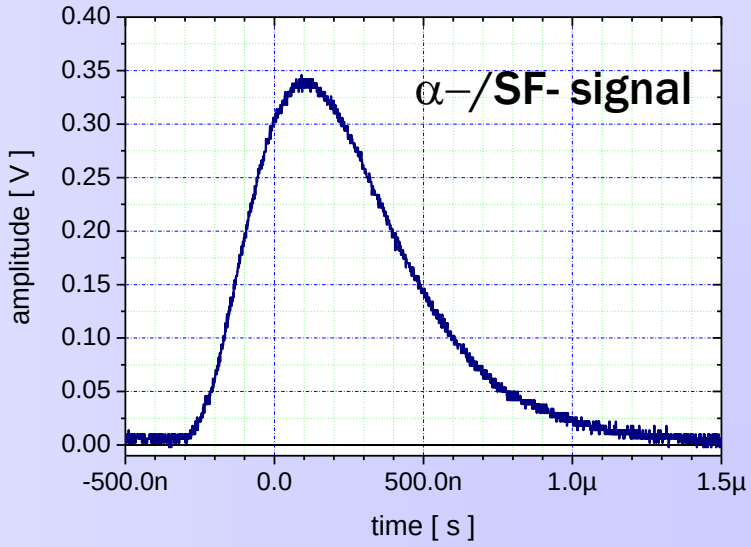
Frontend PCB Design



Preamplifier / Shaper / Amplifier

- pre-amplifier
  - *gain × 10*
  - *shaping time 220 ns*
- main amplifier
  - *separate α- and SF-branch*
  - *fixed gain full range*
    α: 7.5MeV, 15MeV, 30MeV
    SF: 75MeV, 150MeV, 300MeV
  - *fast timing amplifier*
  - *fixed gain full range*
    1.5 MeV, 4.5 MeV, 7.5 MeV
- signal width
  - *375 ns timing signal*
  - *650 ns spectroscopic signal*

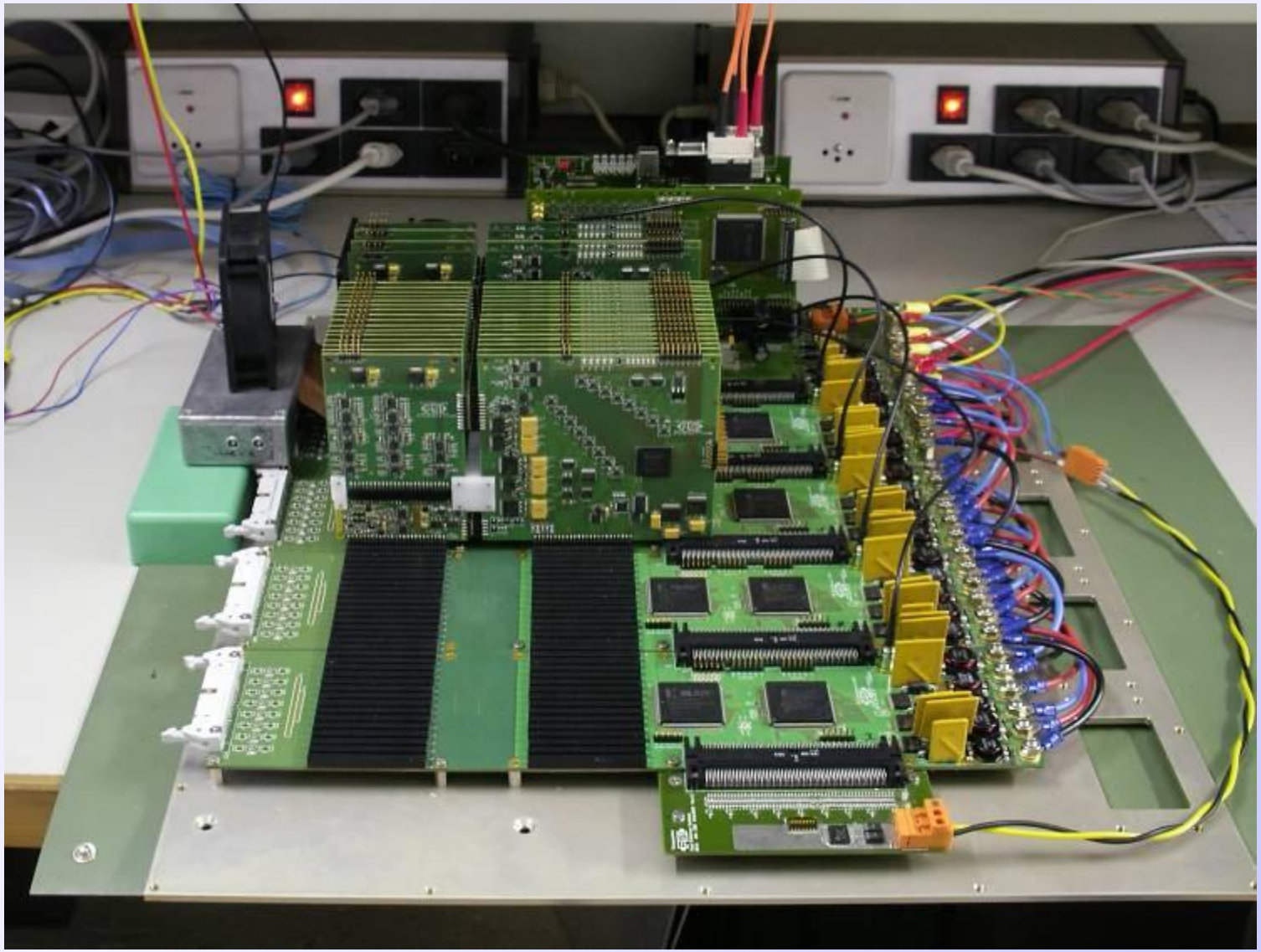




Comparator / ADC / FPGA

- 16 × fast comparators
  - *150 ps switching time 10 ps time jitter*
  - *run-time matching via cable delay better 0.7 ps*
  - *levels adjustable via DAC*
- 8 phase clock
  - *4 × 250 MHz DDR clock*
  - *run-time matching via cable delay better 0.3 ps*
  - *time resolution 0.5 ns*
- 2 × ADC 500 kSamples/s
  - *16 bit conversion depth*
  - *2.5 V bipolar range*
  - *FPGA controlled conversion*
  - *serial data connection*
- Spartan 3 FPGA
  - *16 × counters for fast comparator time- stamps*
  - *2 × ADC readout*
  - *340 Event FIFO*
  - *7x free programmable interconnection signals*

PCB Interconnection Design



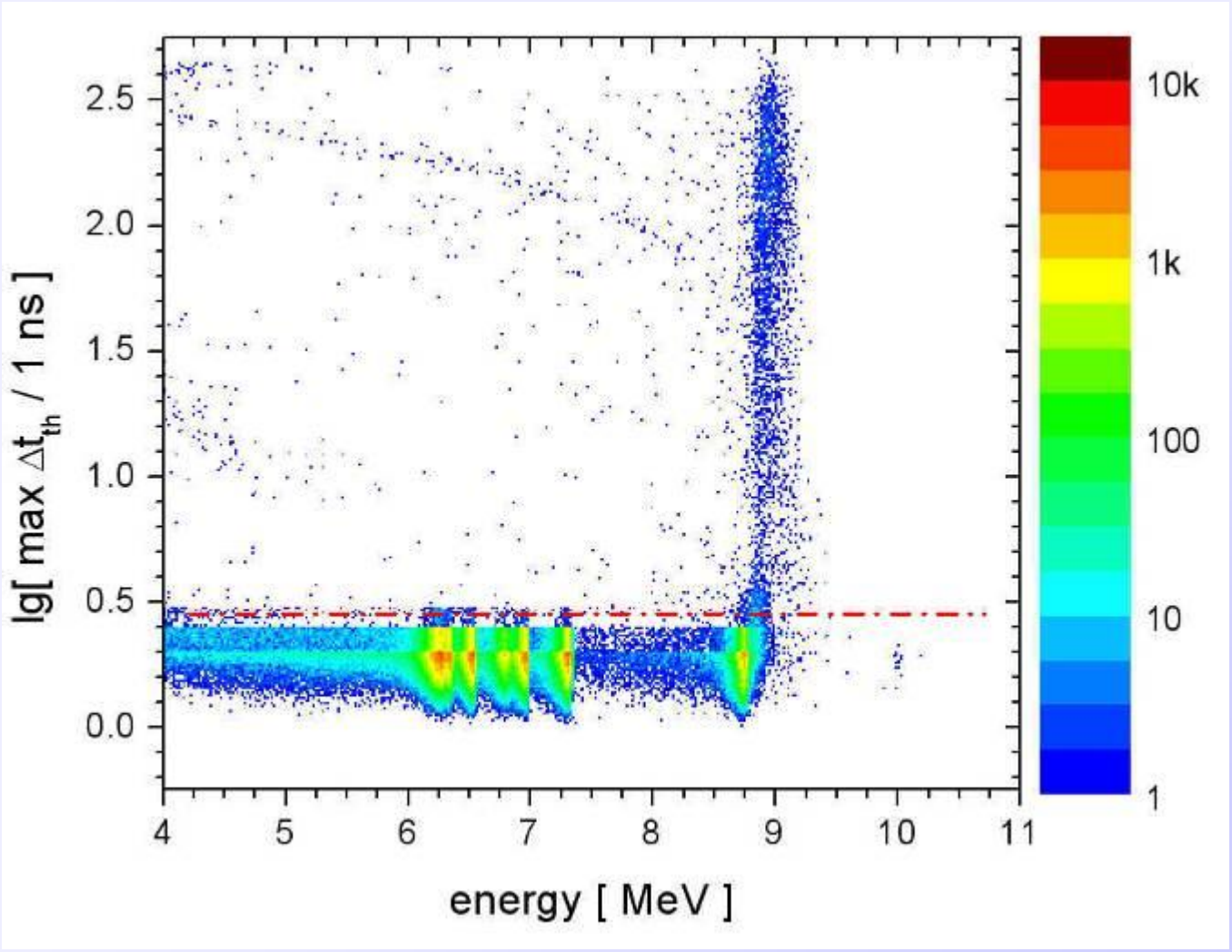
PCB & PC Interconnection

- Main-board
  - *16 × front end PCBs*
  - *Spartan 3 FPGA*
  - *independent read-out for each FE channel*
  - *20 Event FIFO for each FE*
  - *multiplexed test pulse input*
  - *5x free programmable interconnection signals*
- DAC test pulse generator
  - *Fujitsu* MB86064 DAC 14-bit; 800 MSamples/s
  - *2* × free programmable waveforms up to 20.48 *µs*
  - *adjustable reference voltage via 8 bit DAC*
- Interface to PC
  - *Inova GigaSTaR*
  - *point to point bi-directional fiber optics connection*
  - *400 MBit/sec 10 MHz system clock*
  - *max. through put 574 kEvents/sec*
  - *to PC 32 bit data width*
  - *4096 Event FIFO at PC*
  - *from PC 8 bit data width*
  - *Serial interface MCU to PC*
  - *serial ports RS-232 via copper, fiber optics or USB 1.1*

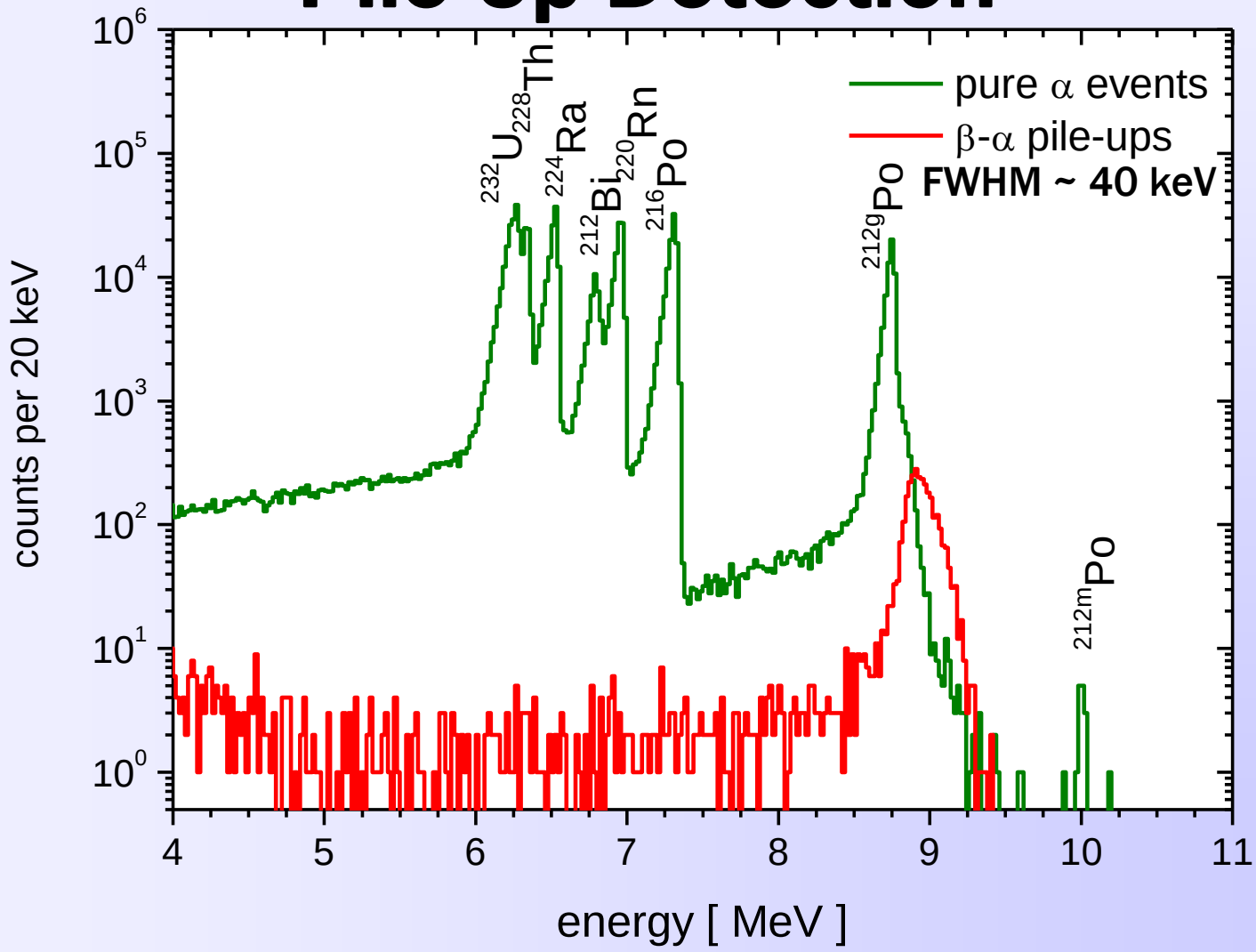
Performance Numbers

- ADC
  - *120 ns conversion time*
  - *1.8 µs transfer to FPGA*
  - *3.1 µs transfer to FIFO*
- Interconnection FE to MB
  - *serial data bus*
  - *all FEs parallel processed*
  - *107 µs transfer time or ~9.4 kEvents/sec*
- Transfer MB to GigaSTaR
  - *32 bit parallel data bus*
  - *1 µs polling over MBs*
  - *12 µs transfer time or 83.3 kEvents/sec*
- GigaSTaR to PC
  - *400 MBit/sec 10 MHz system clock*
  - *max. through put 574 kEvents/sec*
- Experimental Event rate for 1 channel
  - *simulated α-events*
  - *4 µs time between consecutive events*
  - *peak rate 9.0 kEvents/sec*

^{232}U Test Experiments
Threshold-Time vs. α-Energy



^{232}U Test Experiments
Pile-Up Detection



^{232}U Test Experiments
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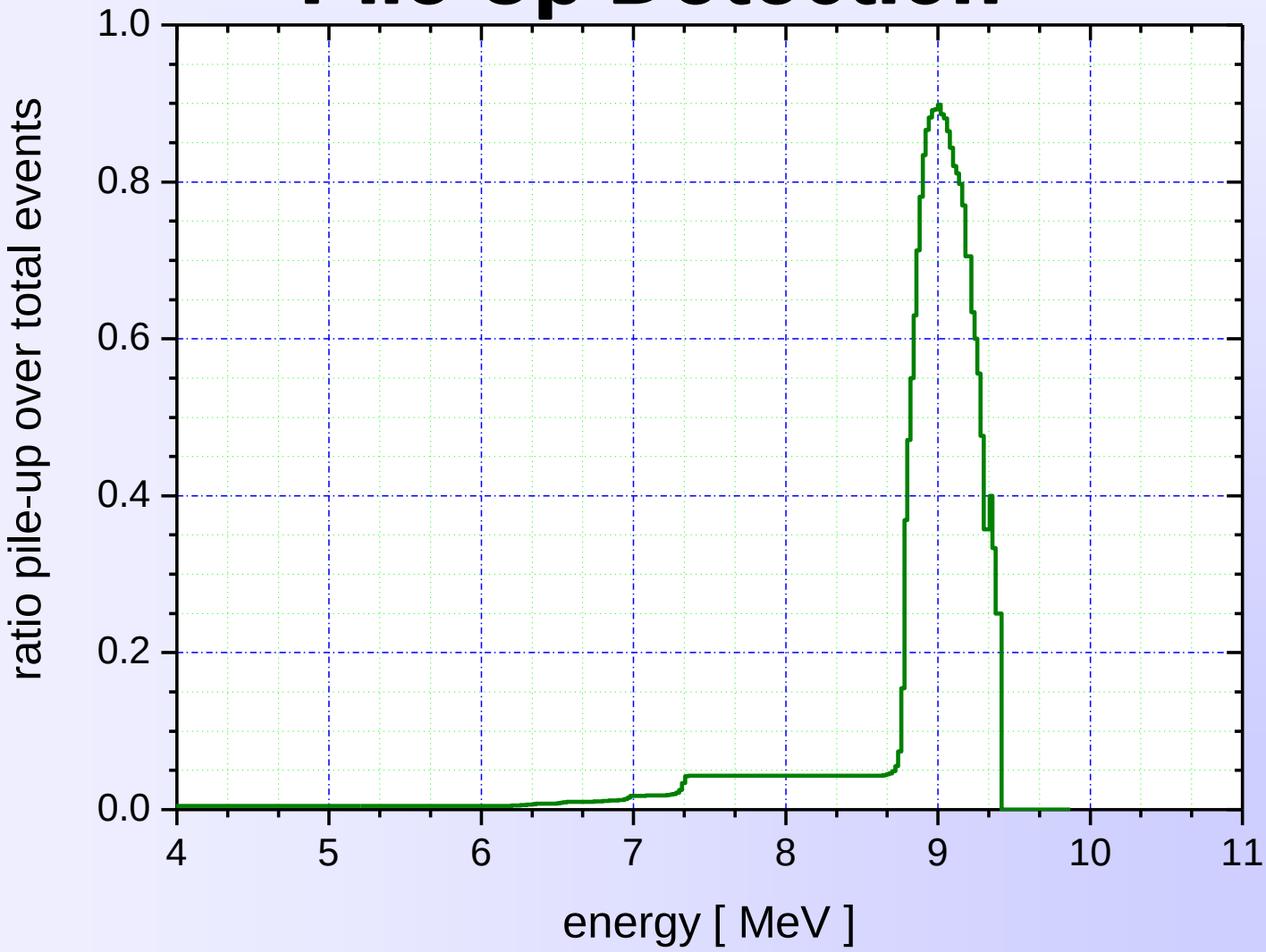
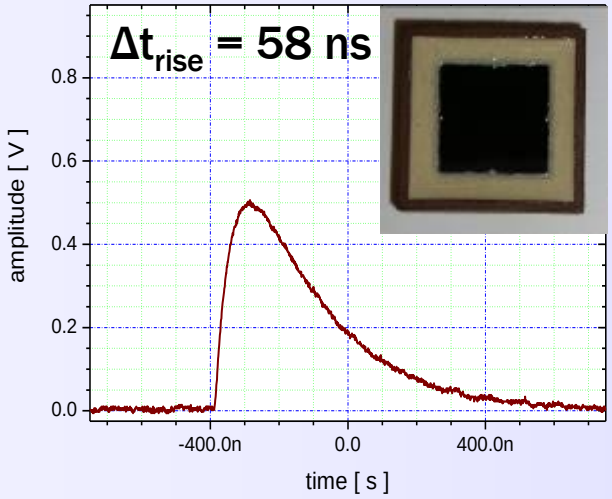
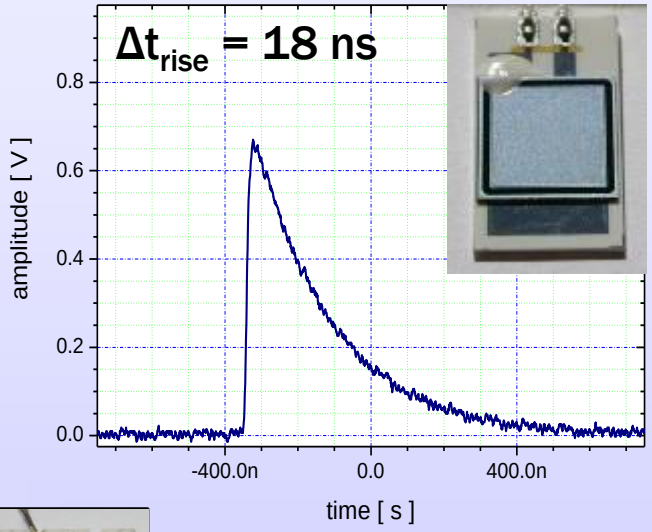
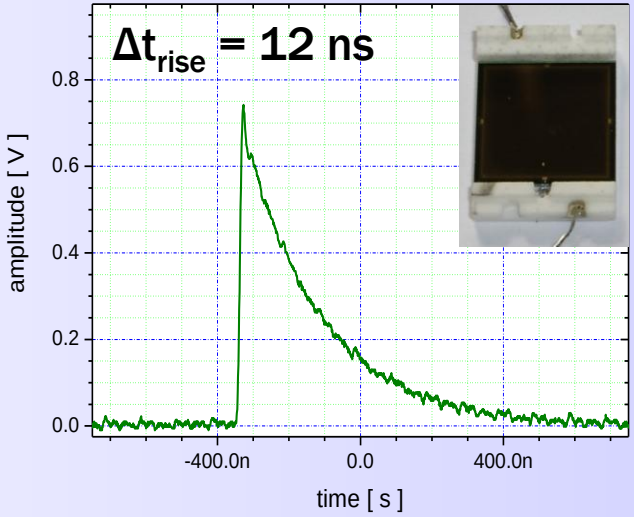


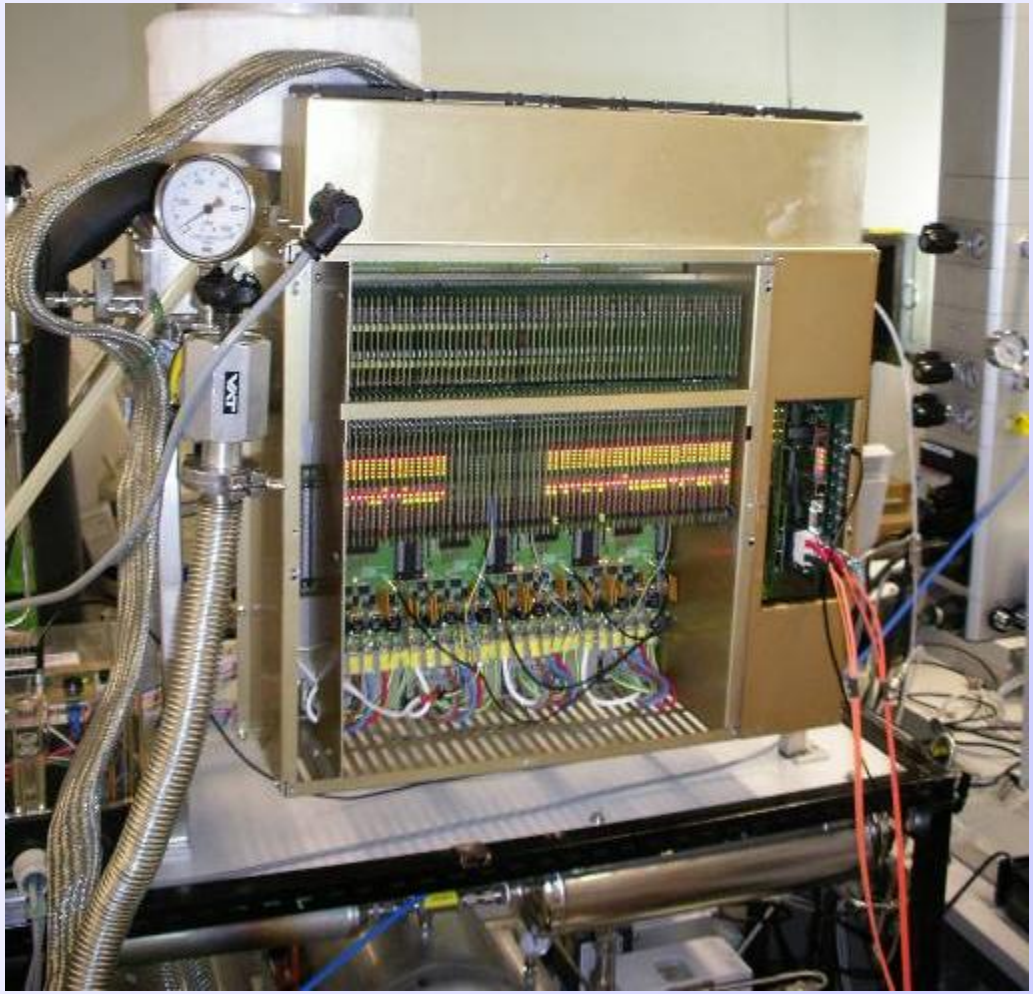
Fast and Slow PIN-Diodes





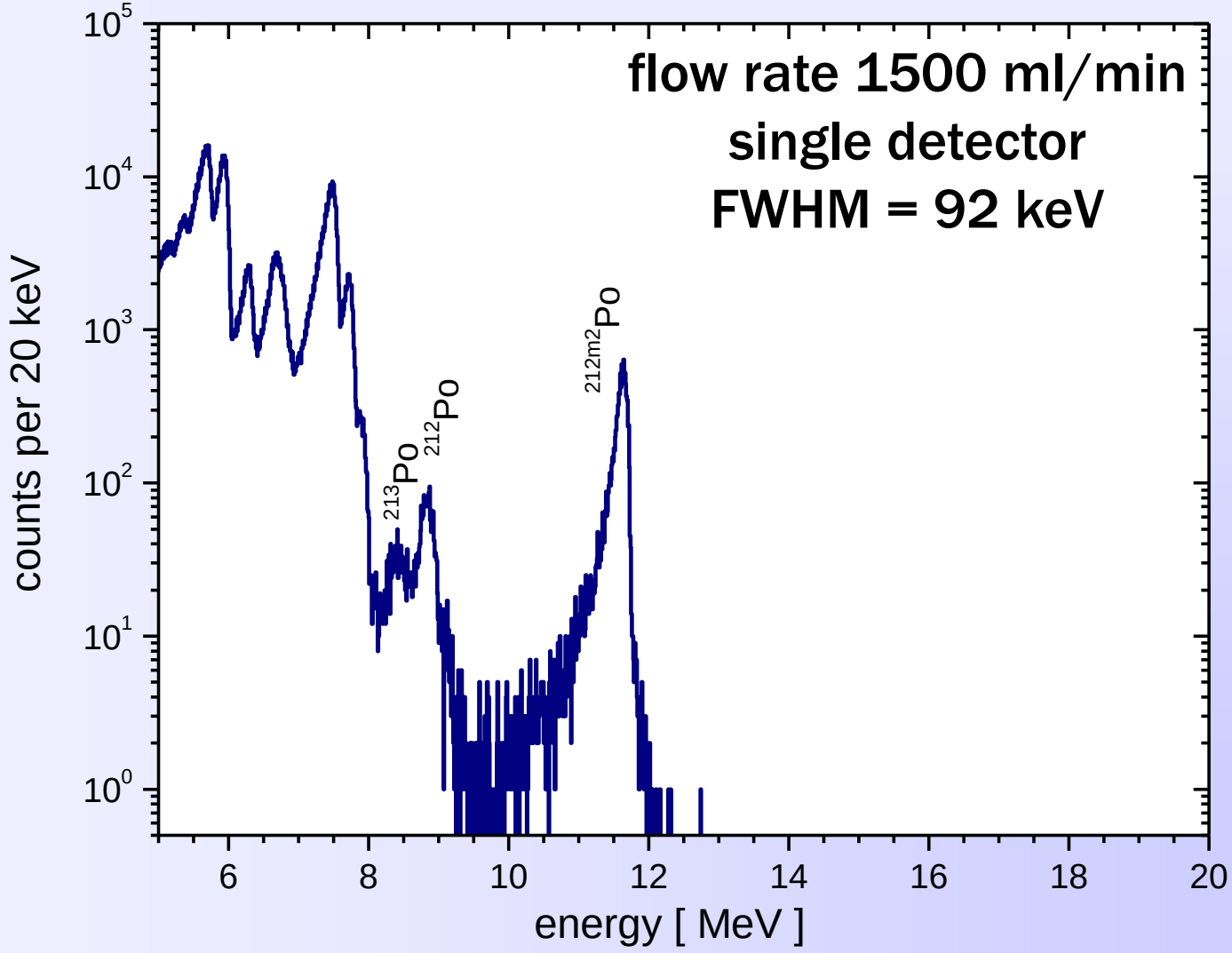


pureCOLD
mounted for on-line experiments



Dubna 2011

$^{244}Pu + ^{48}Ca$



Dubna 2011

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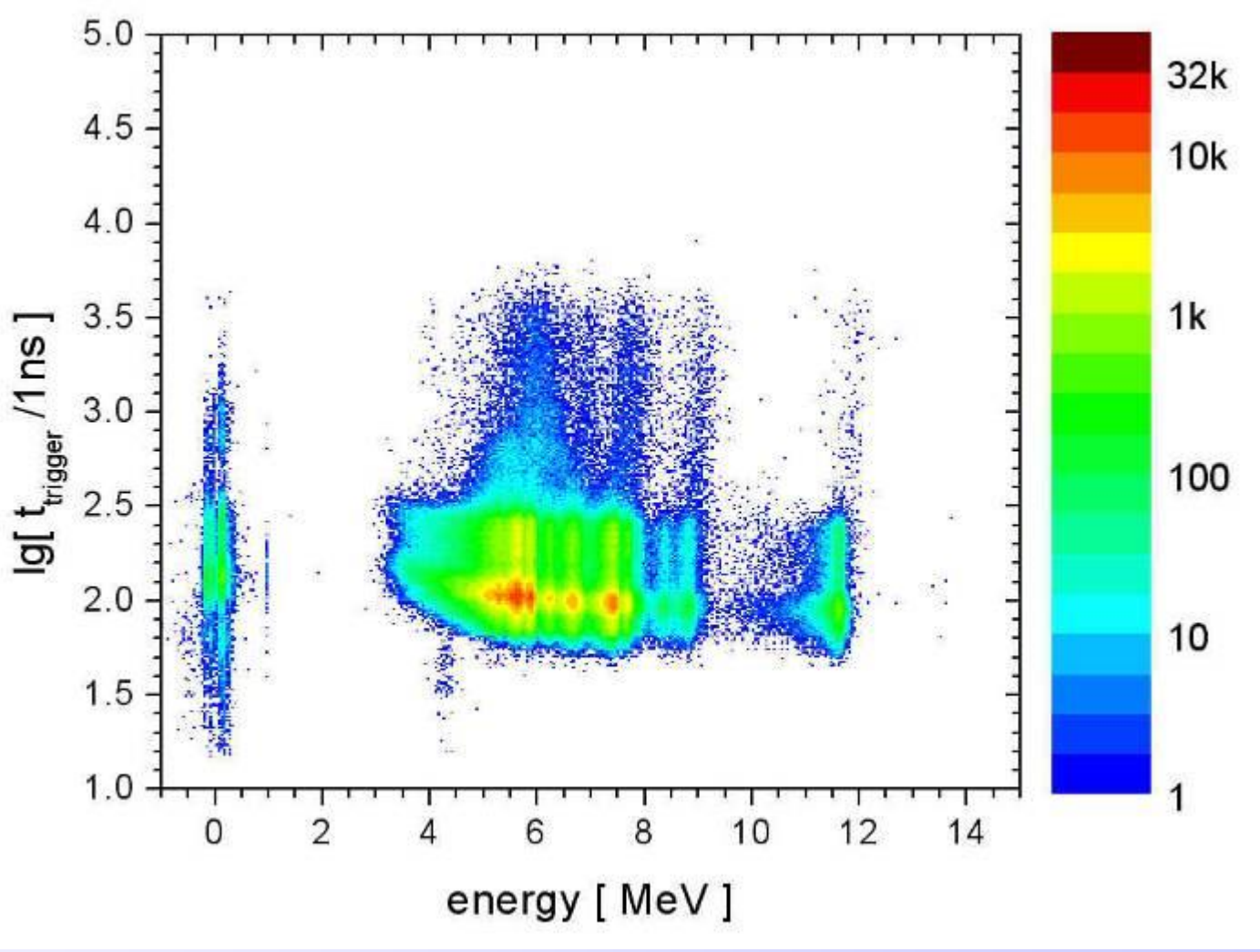
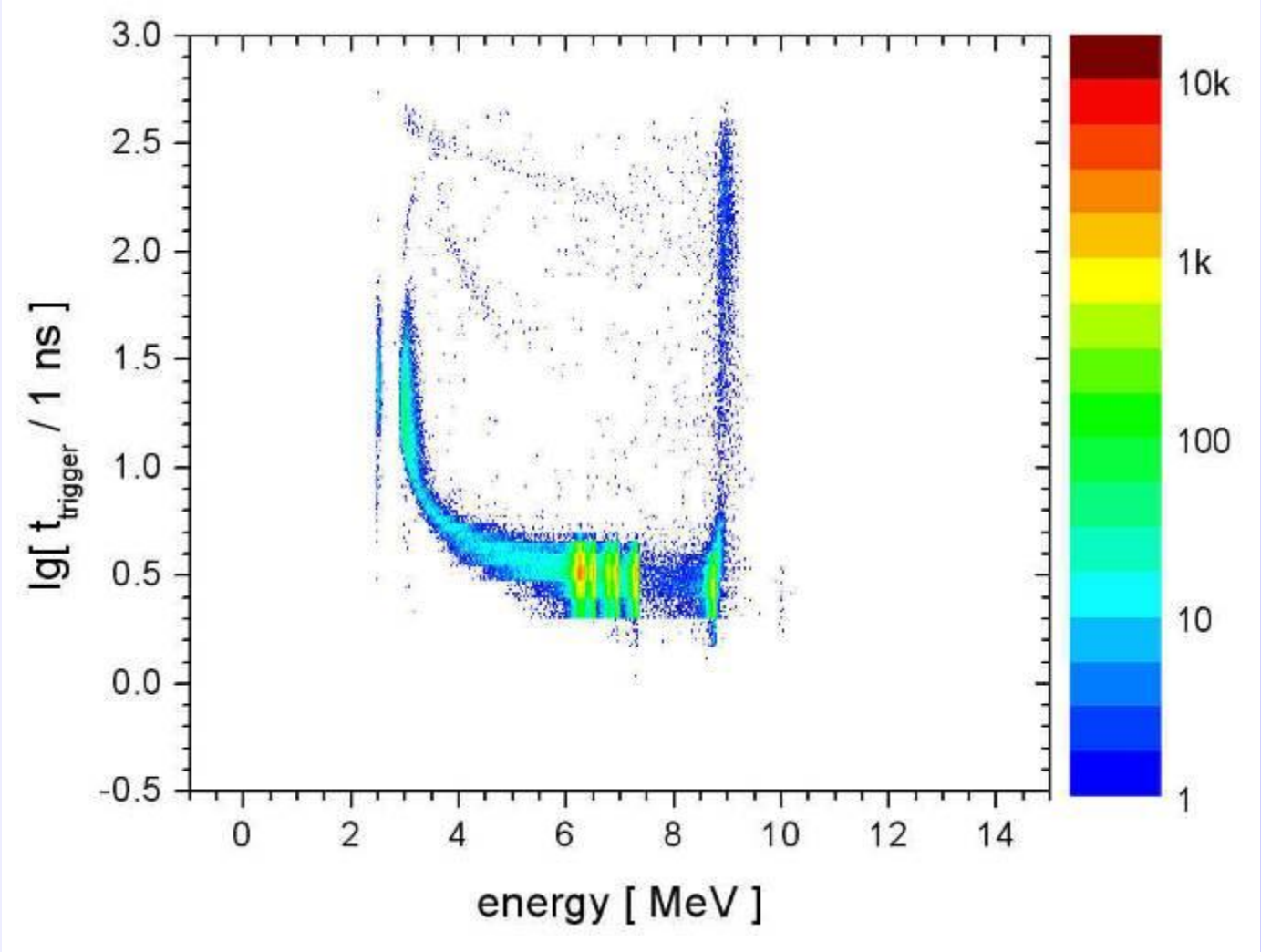
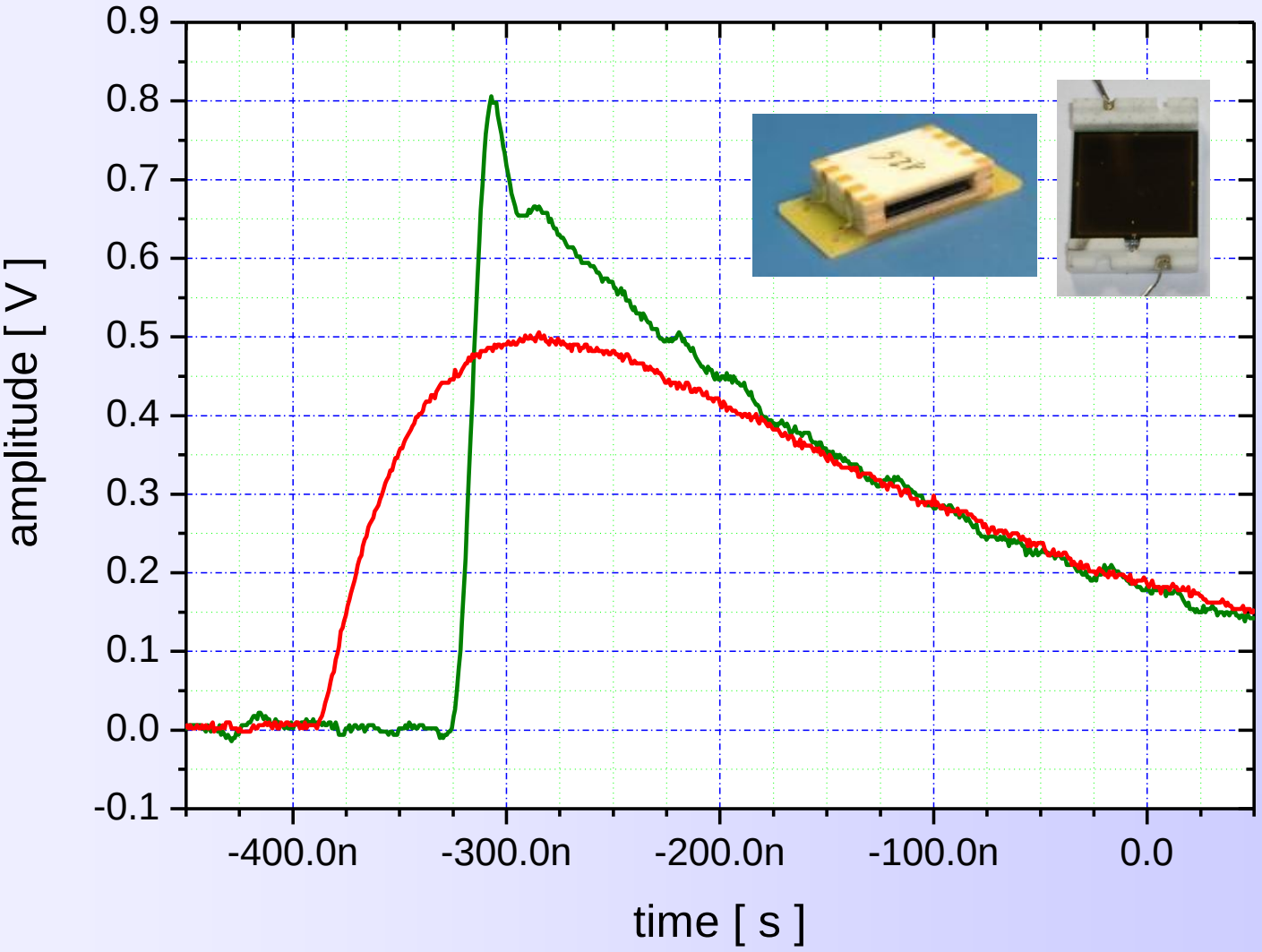


Test at PSI

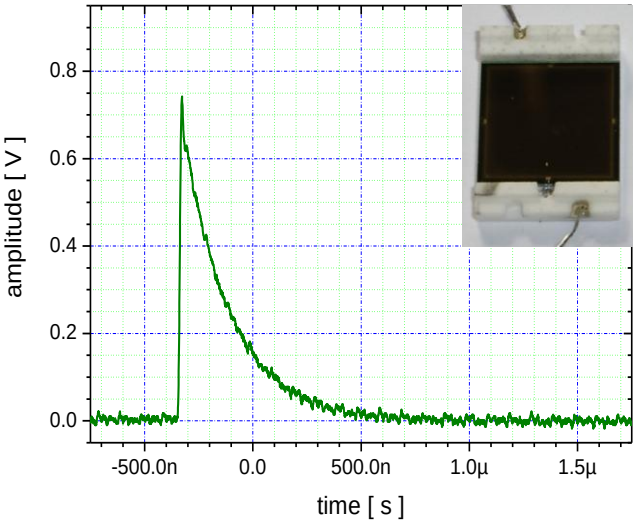

3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
lg[t_trigger / 1 ns]
0
2
4
6
8
10
12
14
energy [MeV]
10k
1k
100
10
1

Fast and slow Signals

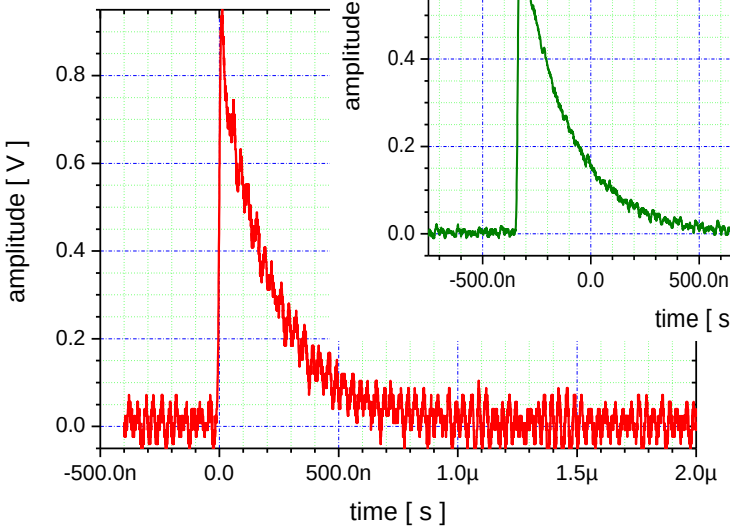


Signal Noise

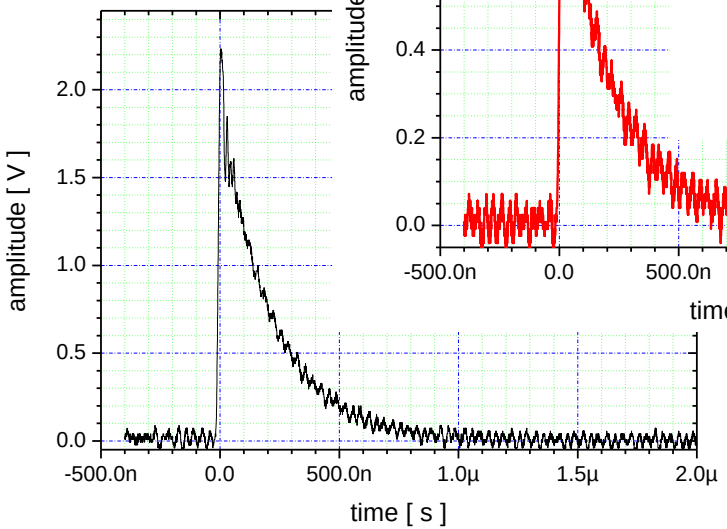
PSI COLD test setup



Dubna COLD



Dubna COLD



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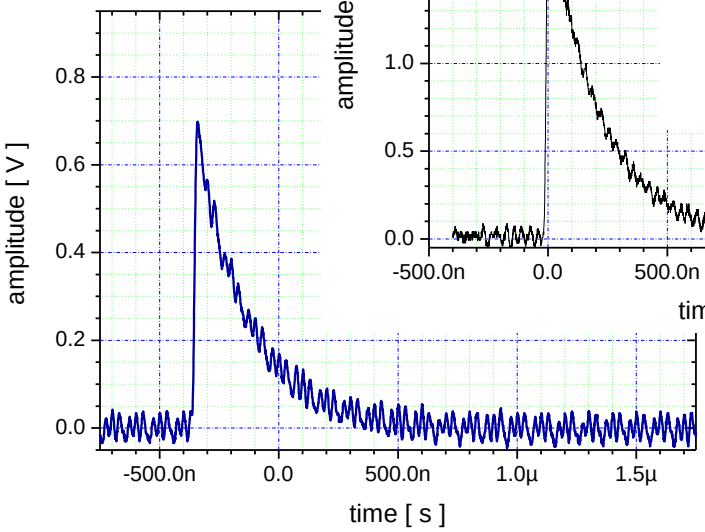

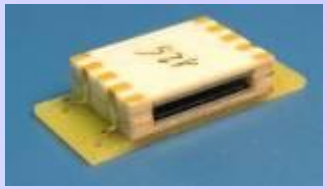

Summary

- good spectroscopic behavior in test experiments
  - *4 µs minimal time between events*
  - *FWHM ~ 40 keV*
  - *pile-up identification about 90%*
- spectroscopic behavior in on-line use
  - *pureCOLD is ready for on-line experiments*
  - *FWHM ~ 90 keV (single detector)*
  - *FWHM ~ 120 keV (all COLD detectors)*

Outlook

- Tuning interconnections
  - *safe transfer protocol FE – MB – GigaSTaR*
  - *use full speed of GigaStaR 1.32 GBit/sec*
    max. through put 1.85 MEvents/sec
- Improvements of FE hardware
  - *max. full range of fast timing amplifier 15 MeV*
  - *noise reduction of analog signals*
  - *rise time problem of PIN-diodes*
- Improvements of FE FPGA-configurations
  - *leading edge detection of threshold passing*
  - *fast counter implementation for threshold time stamp*

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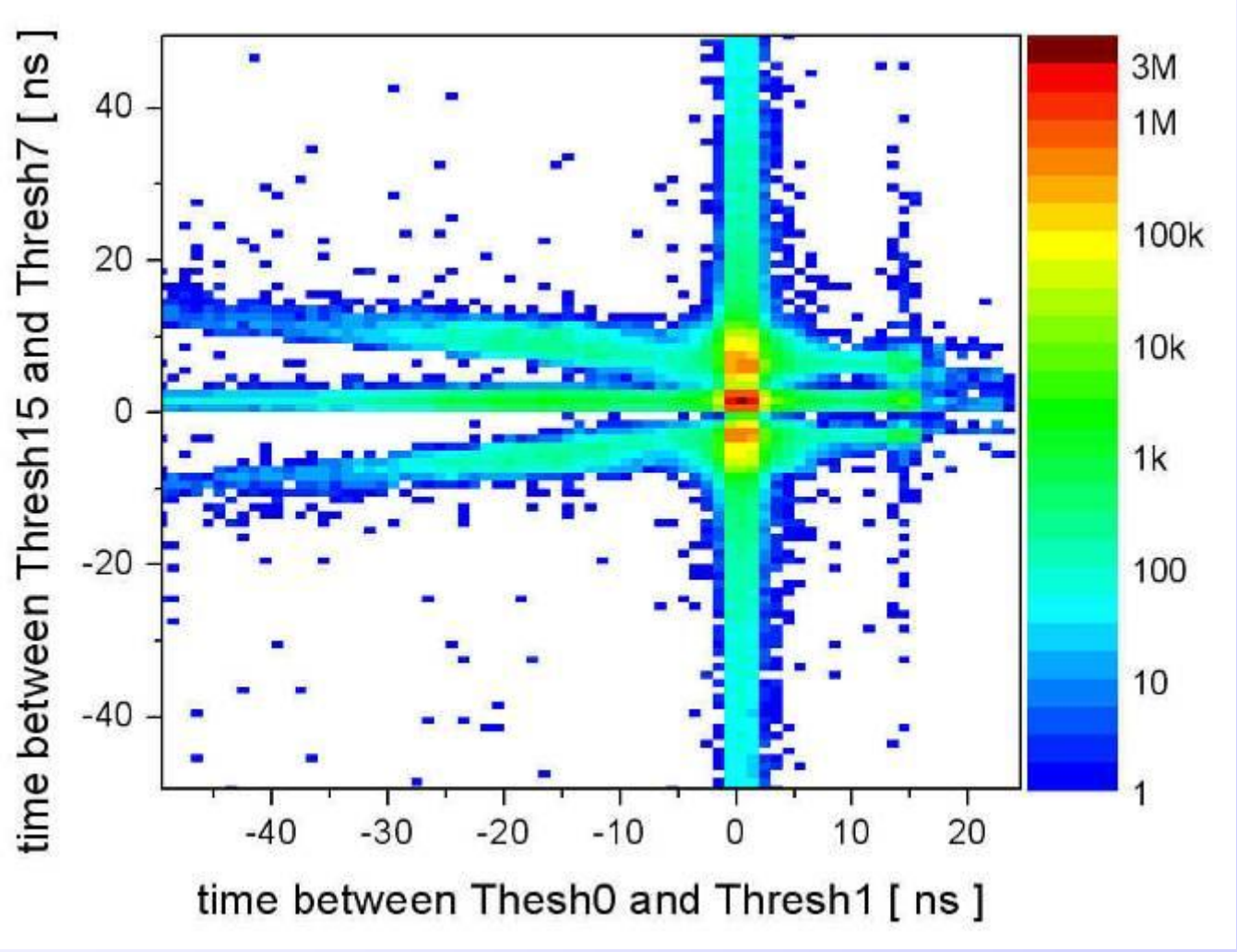
PSI

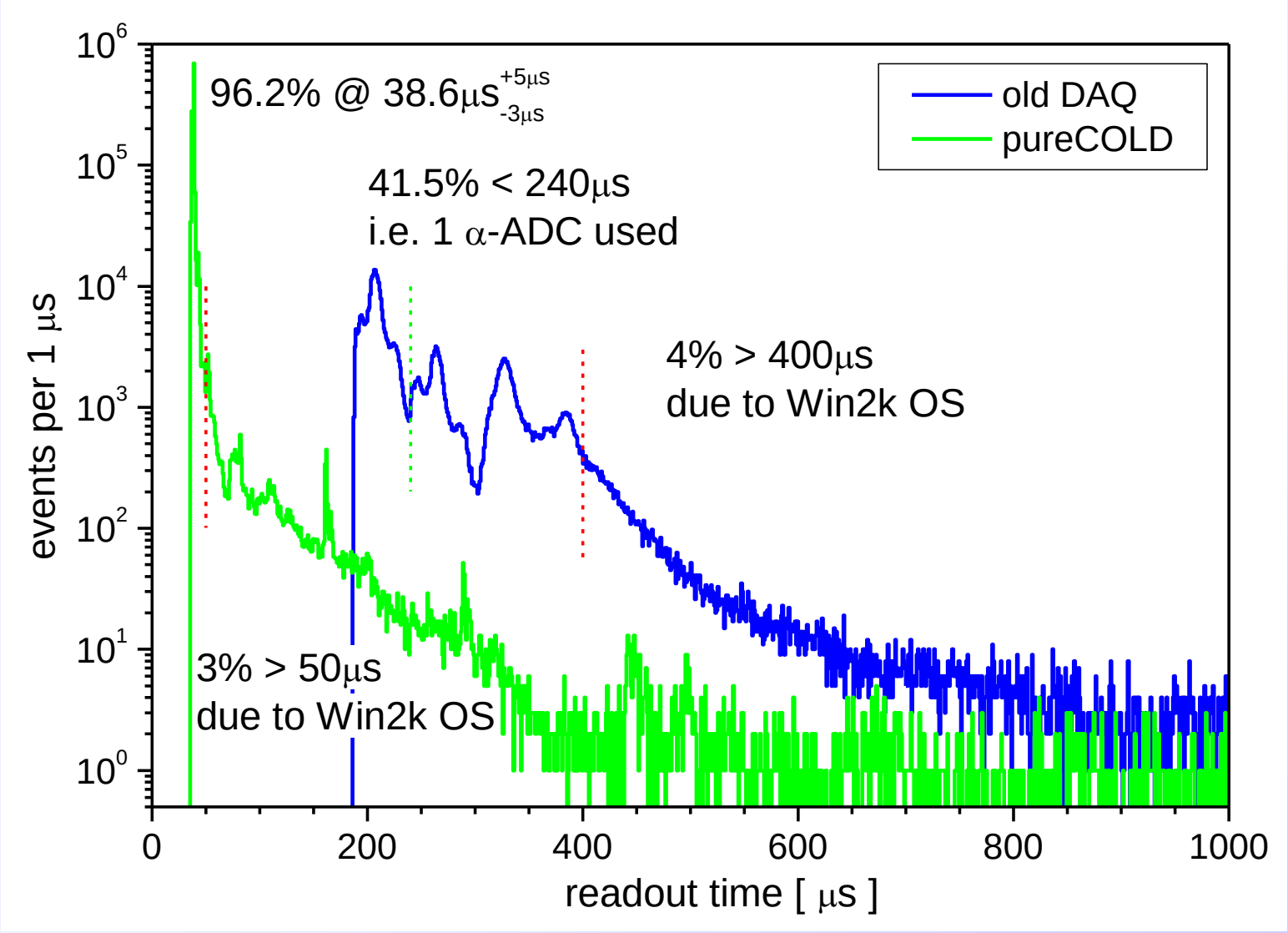
Thank you for your attention

Time between identical Threshold Voltages

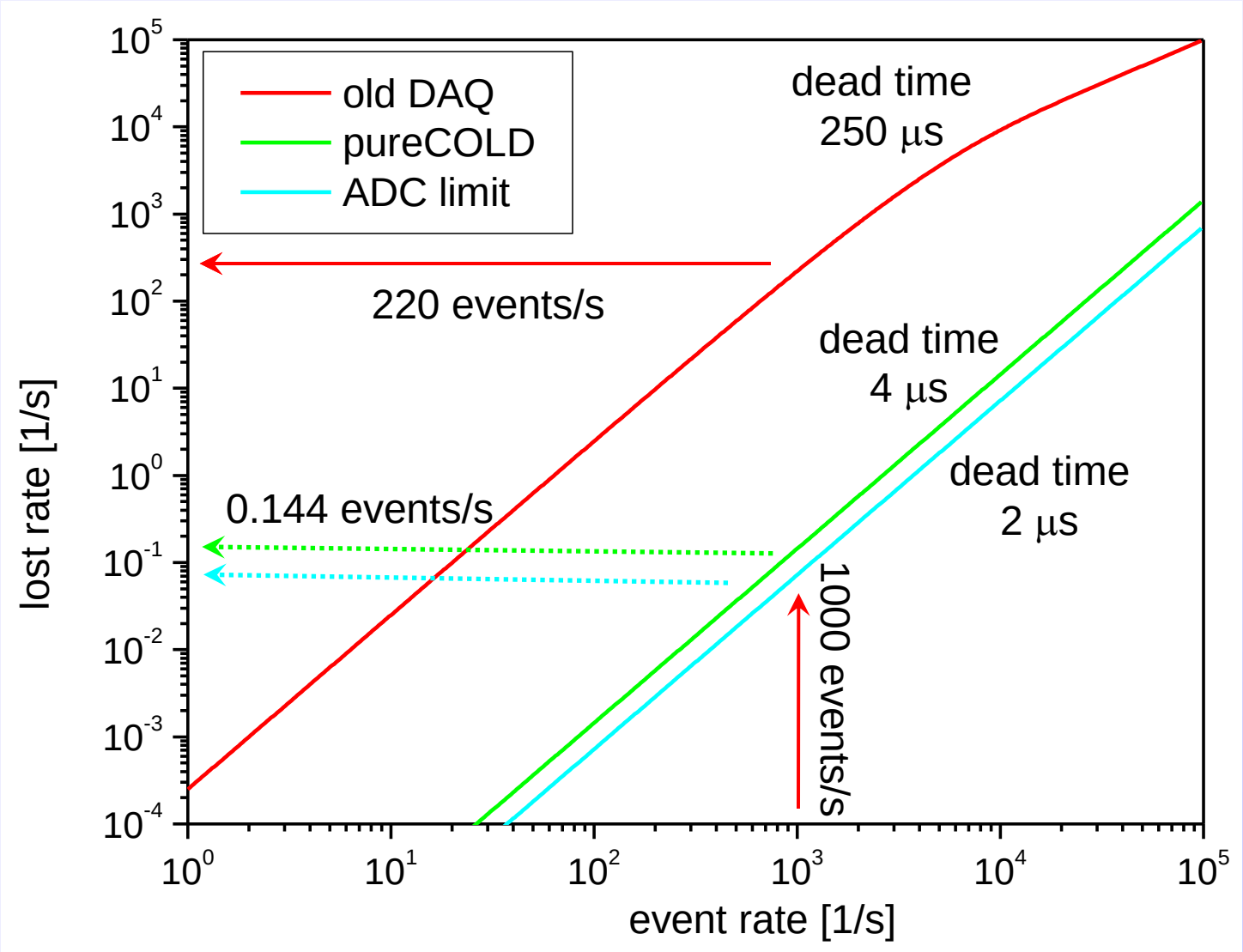


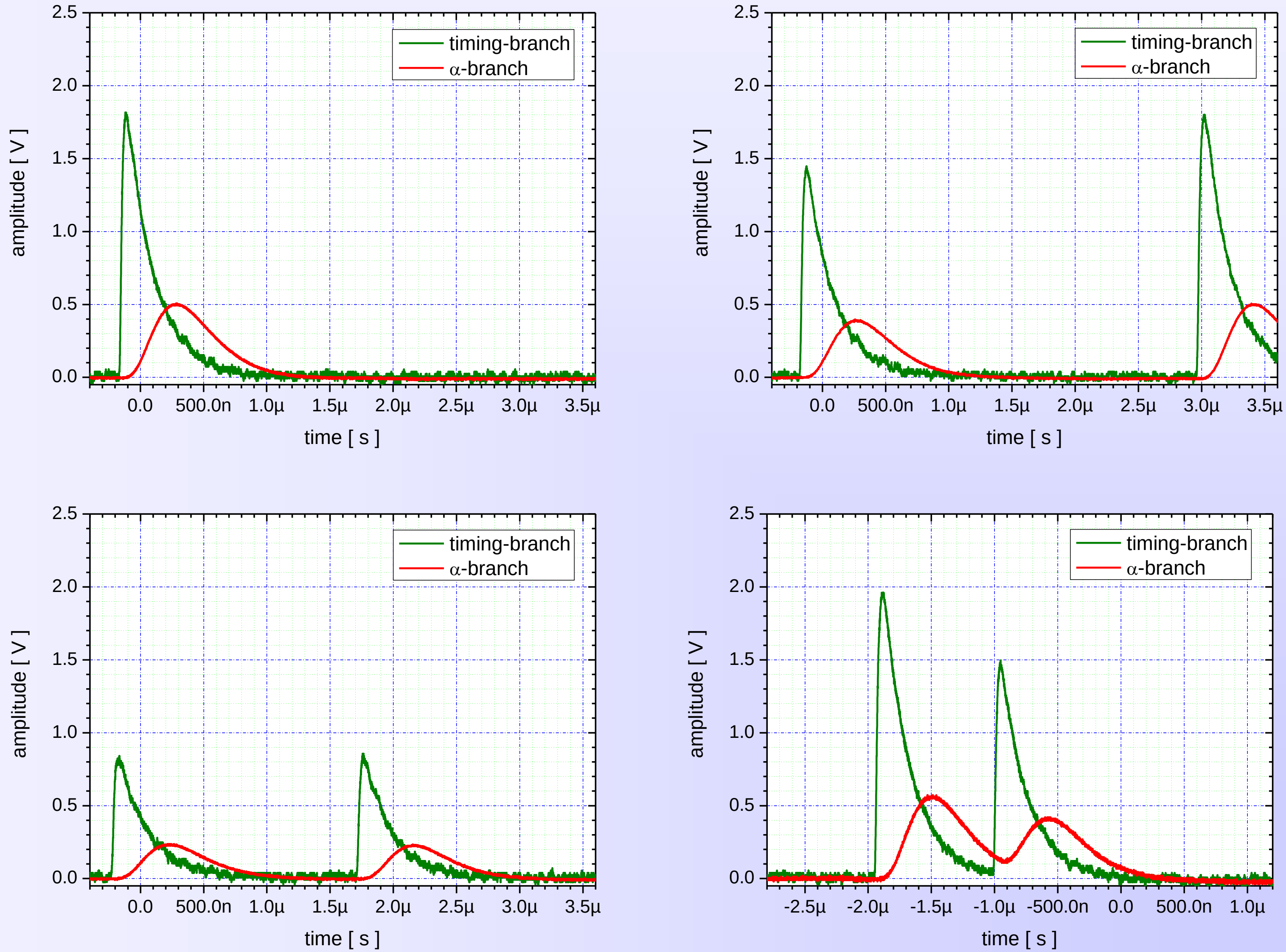
Th#	Level [mV]
15	1000.00
11	2401.96
13	2196.08
12	2000.00
11	1500.00
10	598.04
9	401.96
8	196.08
7	1000.00
6	89.04
5	78.43
4	49.02
3	29.91
2	20.15
1	9.77
0	9.77

Readout Time Spectrum



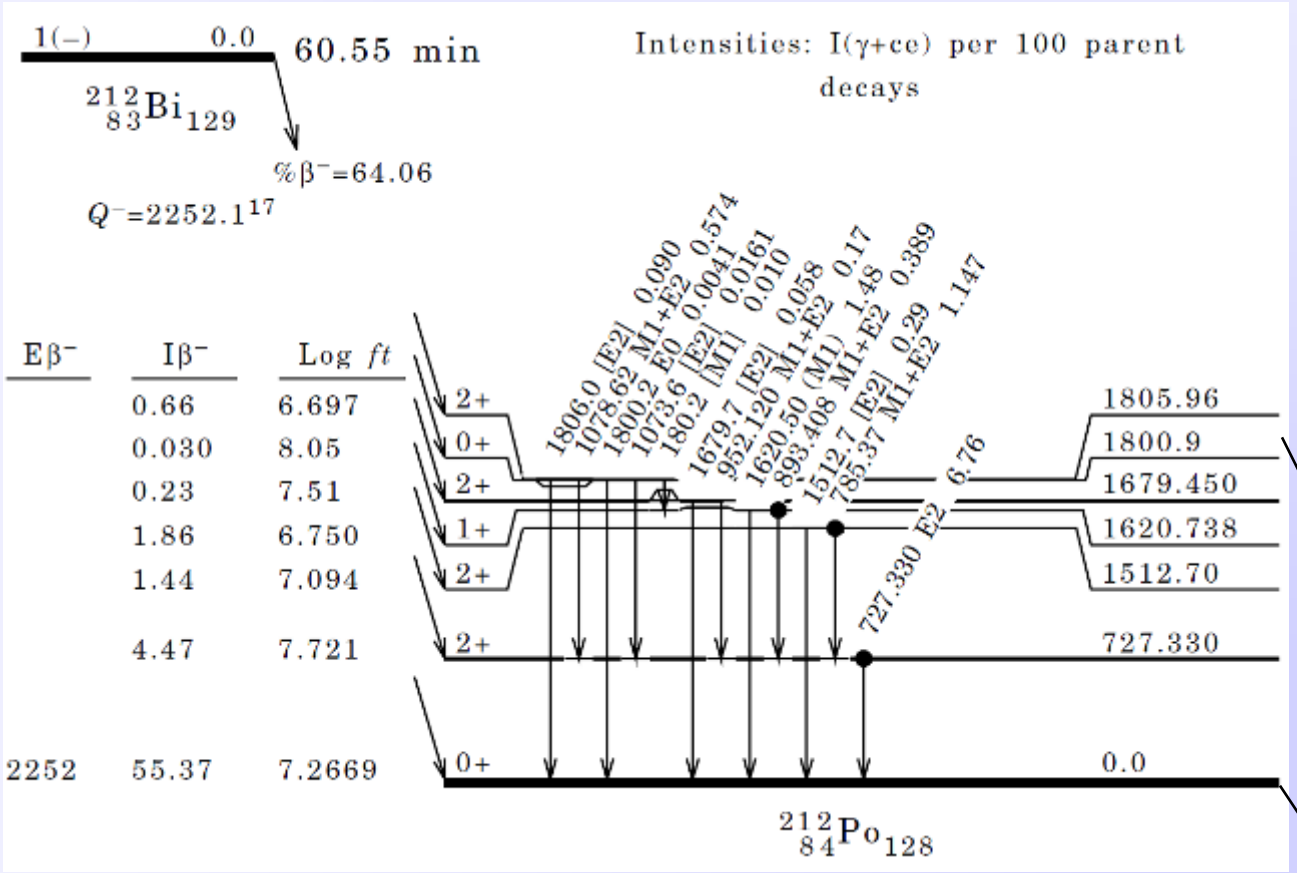
Event Lost Rate





timing-branch
α-branch
amplitude [V]
time [s]
0.0
0.5
1.0
1.5
2.0
2.5
0.0
500.0n
1.0µ
1.5µ
2.0µ
2.5µ
3.0µ
3.5µ
-2.5µ
-2.0µ
-1.5µ
-1.0µ
-500.0n

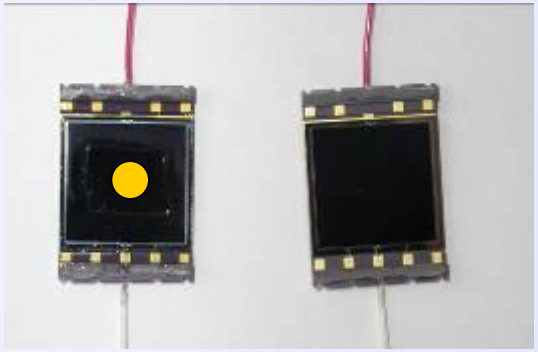
Decay schema of ^{212}Bi

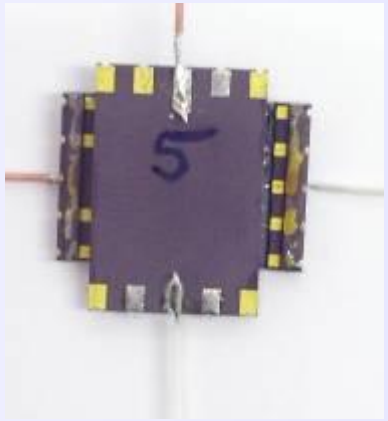


Event Structure

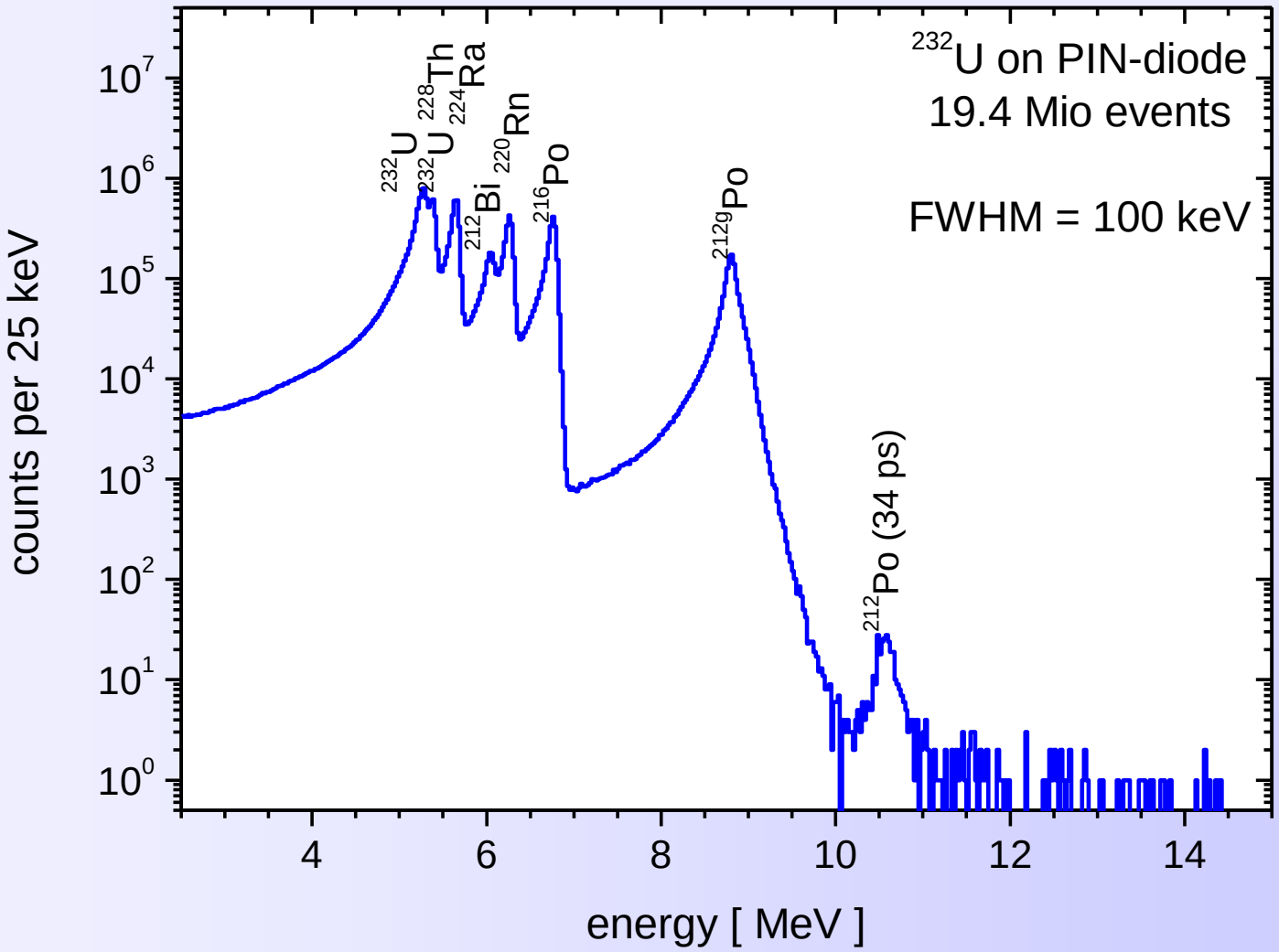
dword	31(MSB)	(LSB)0
1	Event state (16bit)	Event type (8bit) | FE no (8 bit)
2	Alpha ADC conv. time (16bit)	Alpha ADC (16bit)
3	Fiss ADC conv. time (16bit)	Fiss ADC (16bit)
4	Thresh. Time 1 (16bit)	Thresh. Time 0 (16bit)
5	Thresh. Time 3 (16bit)	Thresh. Time 2 (16bit)
6	Thresh. Time 5 (16bit)	Thresh. Time 4 (16bit)
7	Thresh. Time 7 (16bit)	Thresh. Time 6 (16bit)
8	Thresh. Time 9 (16bit)	Thresh. Time 8 (16bit)
9	Thresh. Time 11 (16bit)	Thresh. Time 10 (16bit)
10	Thresh. Time 13 (16bit)	Thresh. Time 12 (16bit)
11	Thresh. Time 15 (16bit)	Thresh. Time 14 (16bit)
18	Beam counter (32bit)	
19	I/O state (16bit)	Beam counter (16bit)
20	Time stamp (32bit)	
21	nn (8bit) | ss (8bit)	Time stamp (16bit)
22	yy (8bit) | mm (8bit) | dd (8bit)	hh (8bit)

First measurements

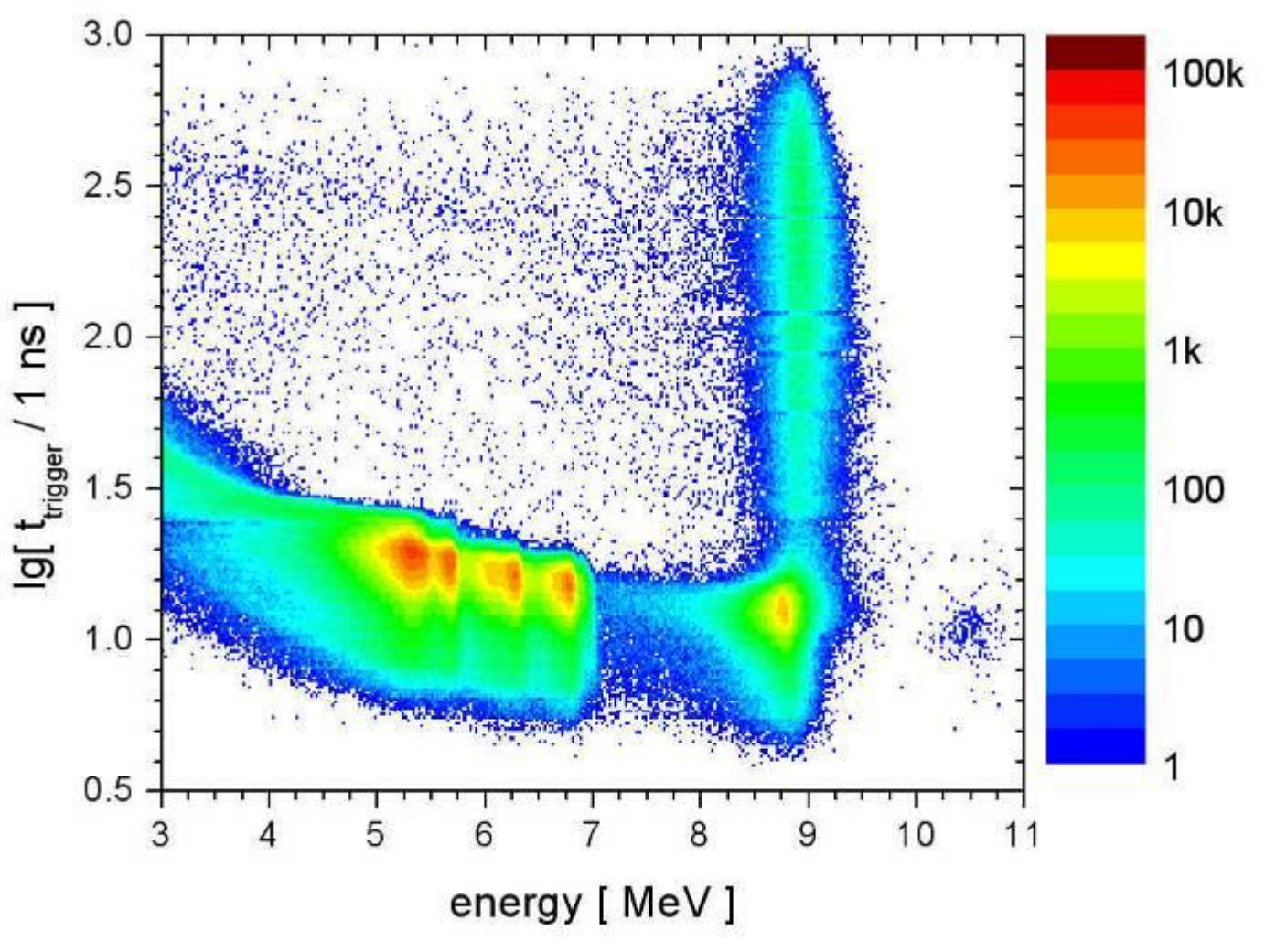




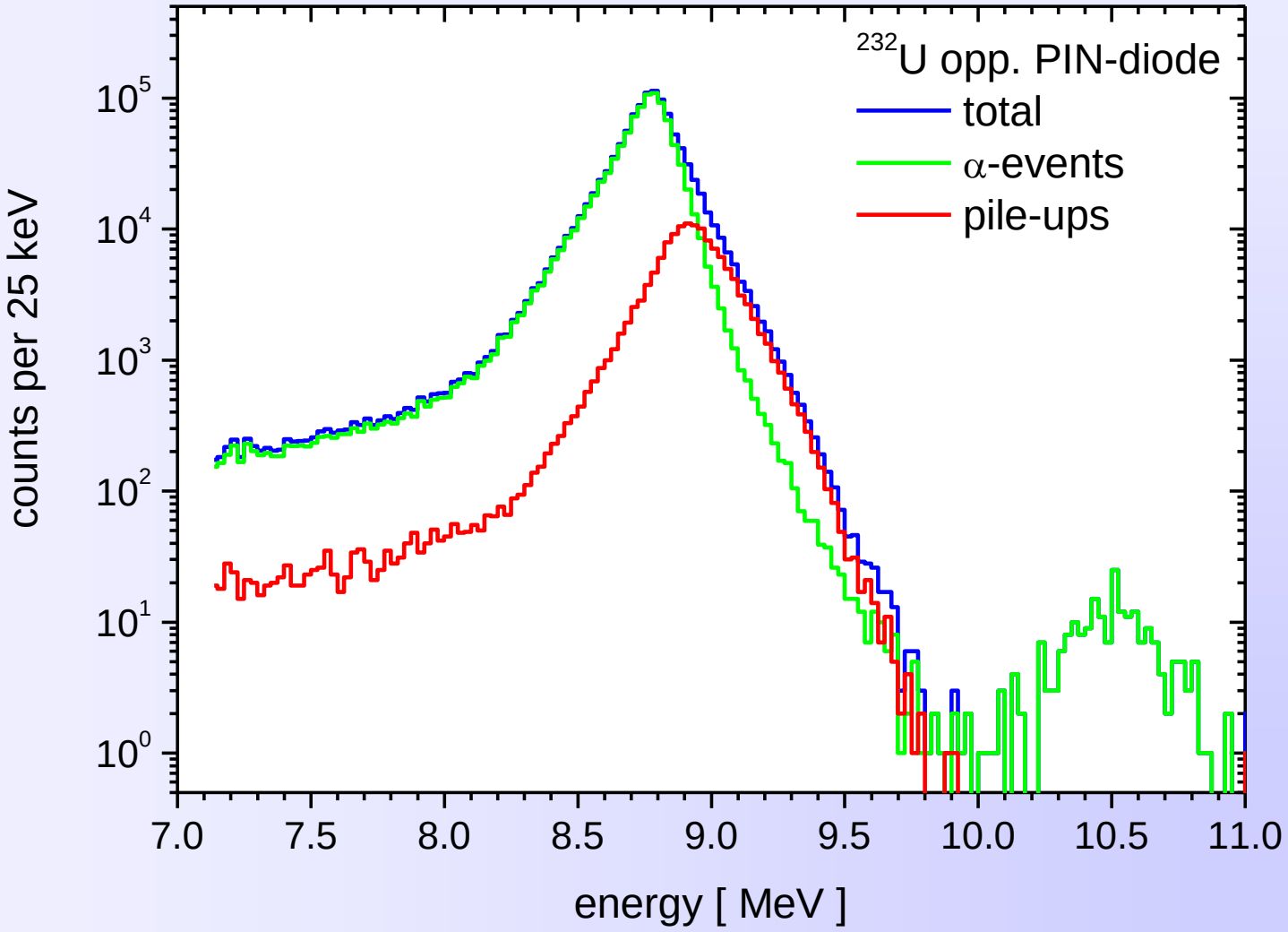
^{232}U α-Spectrum



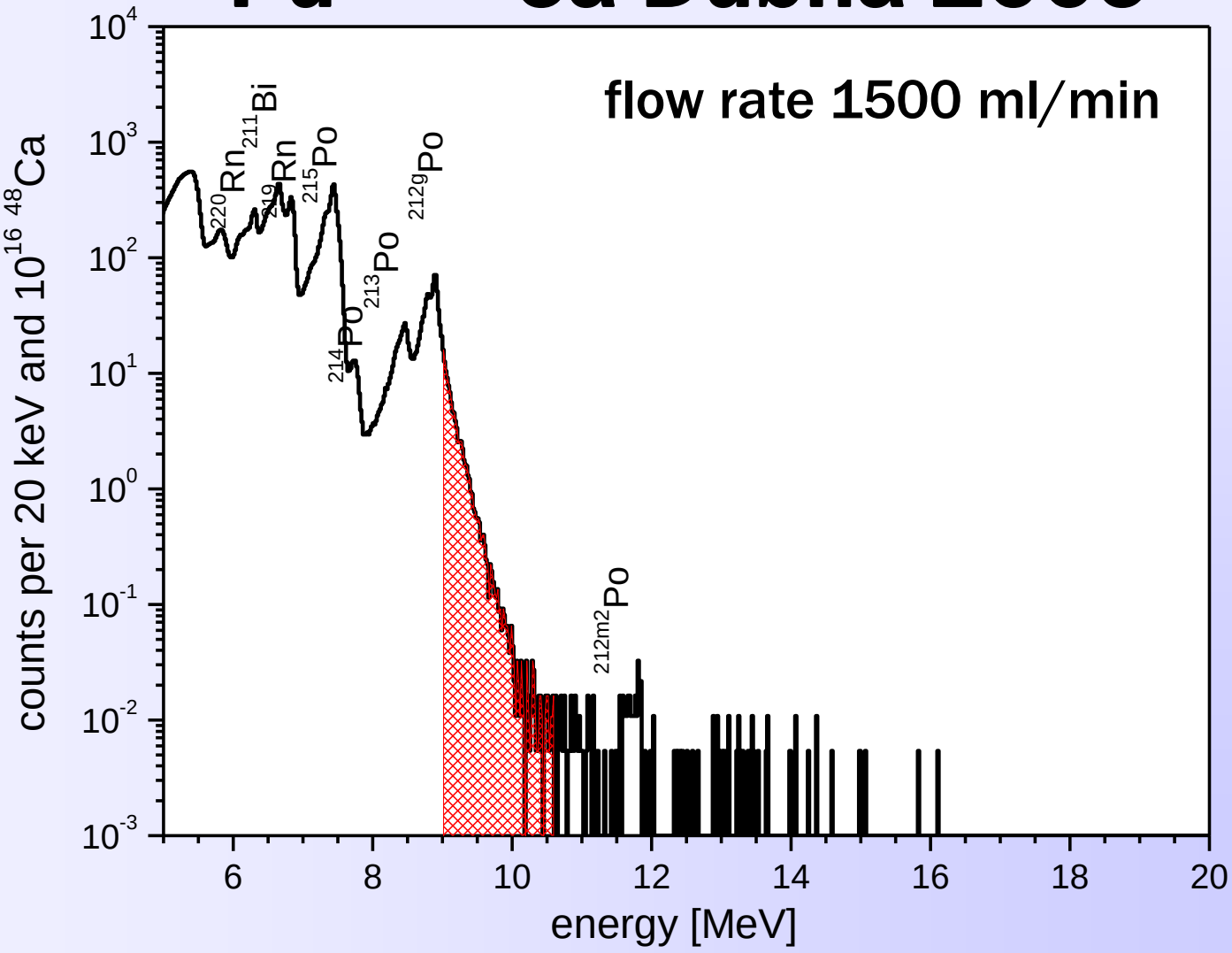
^{232}U Threshold-Time vs. α-Energy



Pile-Up Detection



β-α Pile-up Spectrum
^{242}Pu + ^{48}Ca Dubna 2009



α-α Pile-up Spectrum
^{242}Pu + ^{48}Ca Dubna 2009